R09

Code No: D3704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
COMPUTER AIDED VLSI DESIGN
(CONTROL ENGINEERING)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
- - -

1. Explain Logic verification and logic synthesis.

2. What are the relative advantages and disadvantages of PLA based synthesis and multilevel logic synthesis?

3. Explain Design rule verification.

4. Explain D-Algorithm with example.

5. Explain PODEM algorithm with an example.

6. Consider an example and explain Scan based Testing.

7. Explain Circuit extraction and post layout simulation.

8. Explain Compiled and Event Simulators.

****